

[NAME OF DOCUMENT] Document of abstract

[ABSTRACT]

[PURPOSE]

Providing a semiconductor device with a TFT structure with high reliability

[MEANS]

In a CMOS circuit formed on a substrate 100, a subordinate gate wiring line (a first wiring line) 102a and main gate wiring line (a second wiring line) 107a is provided in an n-channel TFT. The LDD regions 113 overlaps the first wiring line 102a and does not overlap the second wiring line 107a. Thus, applying a gate voltage to the first wiring line forms the GOLD structure, while not applying forms the LLD structure. In this way, the GOLD structure and the LLD structure can be used appropriately in accordance with the respective specifications required for the circuits.

[SELECTED FIGURE] Fig. 1

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## [DESCRIPTION OF A MARK]

101      A substrate  
102a, 102b and 102c      First wiring lines  
103      A first insulating layer  
104 and 105      Active layers  
106      A second insulating layer  
107a, 107b, 107c and 107d      Second wiring lines  
(107a1, 107b1, 107c1 and 107d1      First conductive layers  
107a2, 107b2, 107c2 and 107d2      Second conductive layers  
107d3      A third conductive layer)  
108      A first interlayer insulating layer  
109~111      Third wiring lines  
(109, 110      Source wiring lines  
111      A drain wiring line)

201      A substrate  
202a, 202b and 202c      First wiring lines  
203      A first insulating layer  
204      An active layer  
205      A second insulating layer  
206a, 206b and 206c      Second wiring lines  
(206a1, 206b1 and 206c1      First conductive layers  
206a2, 206b2 and 206c2      Second conductive layers  
206a3      A second conductive layer)  
207      A capacitor wiring line  
(207a      A first conductive layer  
207b      A second conductive layer)  
208      A first interlayer insulating layer  
209      A source wiring line  
210      A drain wiring line  
211      A second interlayer insulating layer  
212      Black masks  
213      A third interlayerinsulating layer  
214      A pixel electrode  
215 and 216      Channel formation regions

601 A substrate with an insulating surface  
602 A pixel matrix circuit  
603 A source driver circuit  
604 A gate driver circuit  
605 A signal processing circuit  
606 An FPC  
1007 An opposite substrate

701 A pixel matrix circuit  
702a and 703a Shift register circuits  
702b and 703b Level shifter circuits  
702c and 703c Buffer circuits  
703d A sampling circuit  
704 A precharge circuit

2001 A main body  
2002 An audio output unit  
2003 An audio input unit  
2004 A display device  
2005 Operation switches  
2006 An antenna

2101 A main body  
2102 A display device  
2103 An audio input unit  
2104 Operation switches  
2105 A battery  
2106 An image receiving unit

2201 A main body  
2202 A camera unit  
2203 An image receiving unit  
2204 Operation switches  
2205 A display device

2301 A main body

2302      Display devices  
2303      Arm units

2401      A main body  
2402      A light source  
2403      A display device  
2404      A polarization beam splitter  
2405      Reflector  
2406      Reflector  
2407      A screen

2501      A main body  
2502      A light source  
2503      A display device  
2504      An optical system  
2505      A screen

[BRIEF DESCRIPTION OF THE FIGURES]

[Fig. 2](A)      A pixel TFT portion  
                  A storage capacitor portion  
          (B)      A storage capacitor portion

[Fig. 3](A)      A phosphorus doping step  
          (B)      A boron doping step  
          (C)      A back side exposure step, A phosphorus doping  
                  step

[Fig. 9](A)      A pixel TFT portion  
                  A storage capacitor portion  
          (B)      A pixel TFT portion  
                  A storage capacitor portion

[Fig. 10](B)     A pixel TFT portion  
                  A storage capacitor portion

[Fig. 11](B)     A pixel TFT portion  
                  A storage capacitor portion

[Fig. 12](A)     A gettering step by phosphorus  
          (C)      A boron doping step  
          (D)      A back side exposure step, A phosphorus doping

step

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